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PATENT
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Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS : Manoj Khare et al.
SERIAL NO. : 09/749,660
FILED : December 28, 2000
FOR : METHOD AND APPARATUS FOR REDUCING
MEMORY LATENCY IN A CACHE COHERENT
MULTI-NODE ARCHITECTURE
GROUP ART UNIT : 2186
EXAMINER : Tuan V. Thai
ASSIGNEE : INTEL CORPORATION

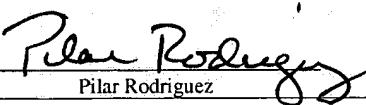
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Dated: April 6, 2004	Signature  Pilar Rodriguez

AMENDMENT

SIR:

The following amendments and remarks below are respectfully submitted in response to the Office Action dated October 6, 2003.